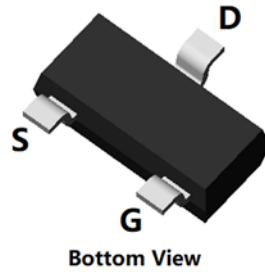
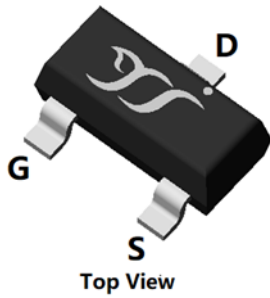
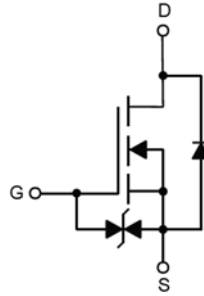


N-Channel Enhancement Mode Field Effect Transistor



SOT-23



Product Summary

- V_{DS} 20V
- I_D 2.5A
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) $< 100m\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=2.5V$) $< 130m\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=1.8V$) $< 200m\Omega$
- ESD Protected Up to 2KV (HBM)

General Description

- High density cell design for Low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 1
- Epoxy Meets UL94 V-0 Flammability Rating
- Halogen Free

Applications

- PWM applications
- Power management
- Load switch

Limiting Values

Parameter	Conditions	Symbol	Min	Max	Unit	
Drain-source Voltage		V_{DS}	-	20	V	
Gate-source Voltage		V_{GS}	-8	8		
Continuous Drain Current (Note 1,2)	Steady-State	I_D	$T_A=25^\circ C, V_{GS}= 10V$	-	2.5	A
			$T_A=100^\circ C, V_{GS}= 10V$	-	1.6	
Pulsed Drain Current	$T_A=25^\circ C, t_p \leq 10\mu s$	I_{DM}	-	10		
Maximum Body-Diode Continuous Current	$T_A=25^\circ C$	I_S		1.1		
Total Power Dissipation (Note 1,2)	Steady-State	P_D	$T_A=25^\circ C$	-	0.93	W
			$T_A=100^\circ C$	-	0.37	
Junction and Storage Temperature Range		T_J, T_{STG}	-55	150	$^\circ C$	

Thermal Resistance

Parameter	Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	$R_{\theta JA}$	-	133	$^\circ C/W$

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL2302AK	F2	S2K	3000	30000	120000	7" reel



YJL2302AJK

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A, T_J=25^\circ C$	20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V, T_J=25^\circ C$	-	-	1	μA
		$V_{DS}=20V, V_{GS}=0V, T_J=150^\circ C$	-	-	100	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 8V, V_{DS}=0V, T_J=25^\circ C$	-	-	± 10	μA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A, T_J=25^\circ C$	0.4	0.7	1.0	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=2A, T_J=25^\circ C$	-	65	100	m Ω
		$V_{GS}=2.5V, I_D=1.5A, T_J=25^\circ C$	-	85	130	
		$V_{GS}=1.8V, I_D=0.5A, T_J=25^\circ C$	-	110	200	
Diode Forward Voltage	V_{SD}	$I_S=2A, V_{GS}=0V, T_J=25^\circ C$	-	0.83	1.2	V
Gate Resistance	R_G	$f=1MHz, T_J=25^\circ C$	-	14	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{DS}=10V, V_{GS}=0V, f=1MHz, T_J=25^\circ C$	-	131	-	pF
Output Capacitance	C_{oss}		-	22	-	
Reverse Transfer Capacitance	C_{riss}		-	11	-	
Switching Parameters						
Total Gate Charge	Q_g	$V_{GS}=4.5V, V_{DS}=10V, I_D=2A, T_J=25^\circ C$	-	1.4	-	nC
Gate-Source Charge	Q_{gs}		-	0.09	-	
Gate-Drain Charge	Q_{gd}		-	0.3	-	
Reverse Recovery Charge	Q_{rr}	$I_F=2A, di/dt=100A/\mu s, V_{GS}=0V, V_R=10V, T_J=25^\circ C$	-	2.3	-	nC
Reverse Recovery Time	t_{rr}		-	7.4	-	ns
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V, V_{DS}=10V, I_D=2A, R_L=5\Omega, R_{GEN}=3\Omega, T_J=25^\circ C$	-	6.4	-	ns
Turn-on Rise Time	t_r		-	22	-	
Turn-off Delay Time	$t_{D(off)}$		-	14	-	
Turn-off Fall Time	t_f		-	3.3	-	

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in² pad of 2oz. Copper, in the still air environment with $T_A=25^\circ C$. The maximum allowed junction temperature of $150^\circ C$. The value in any given application depends on the user's specific board design.
- Thermal resistance from junction to soldering point (on the exposed drain pad).



■ Typical Electrical and Thermal Characteristics Diagrams

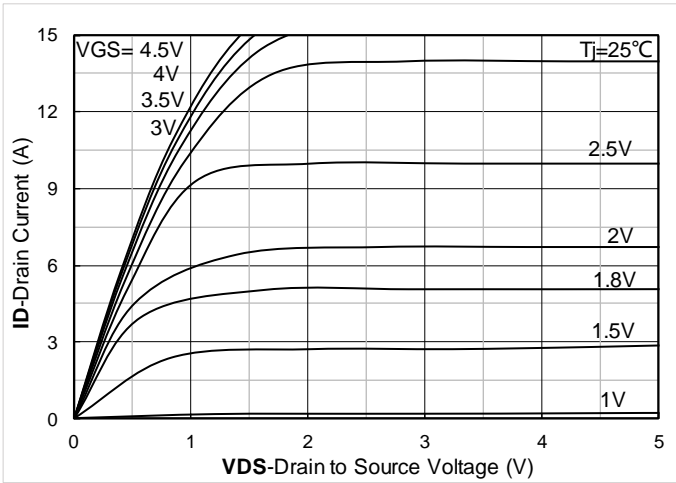


Figure 1. Output Characteristics; typical values

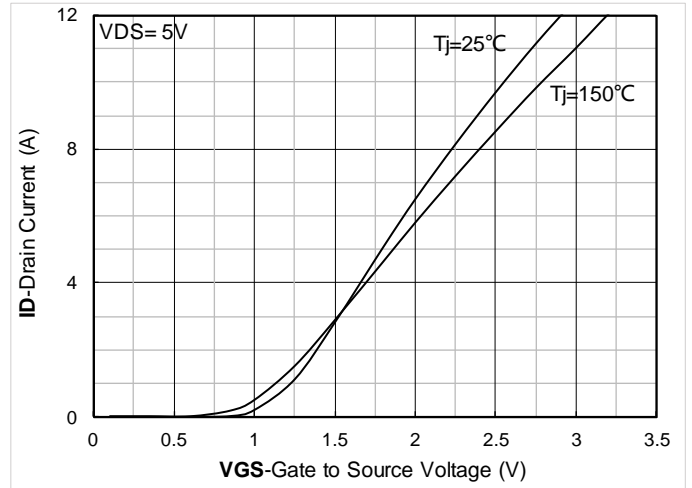


Figure 2. Transfer Characteristics; typical values

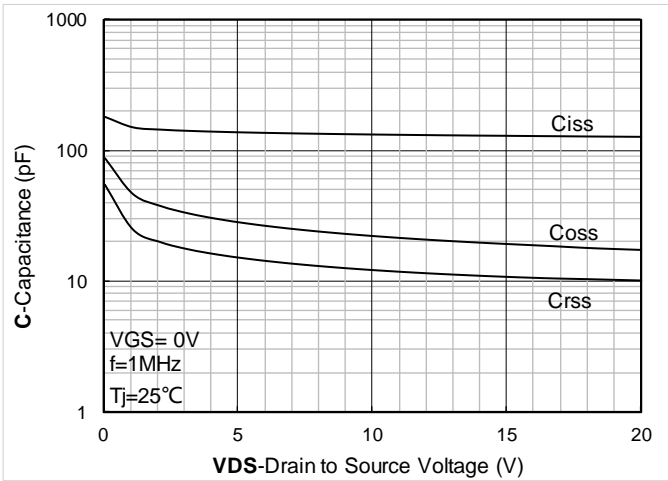


Figure 3. Capacitance Characteristics; typical values

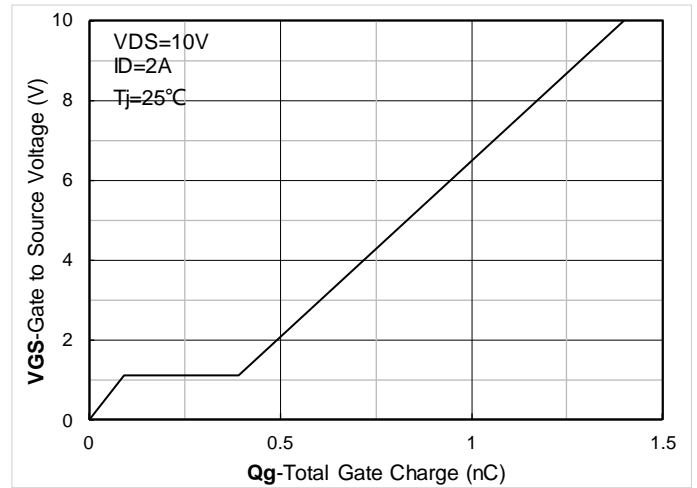


Figure 4. Gate Charge; typical values

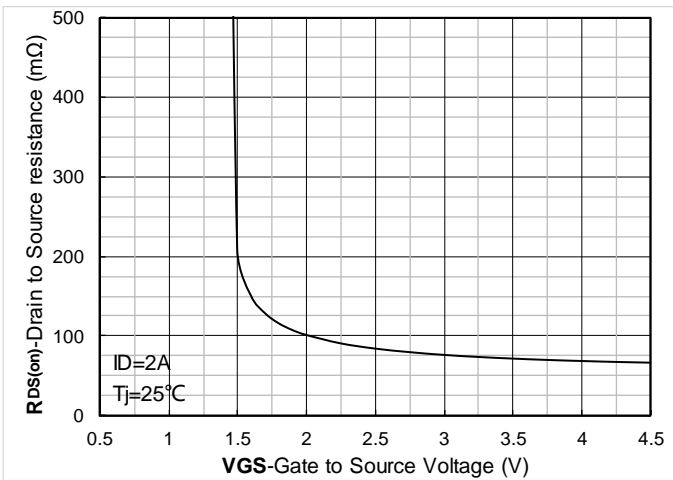


Figure 5. On-Resistance vs Gate to Source Voltage; typical values

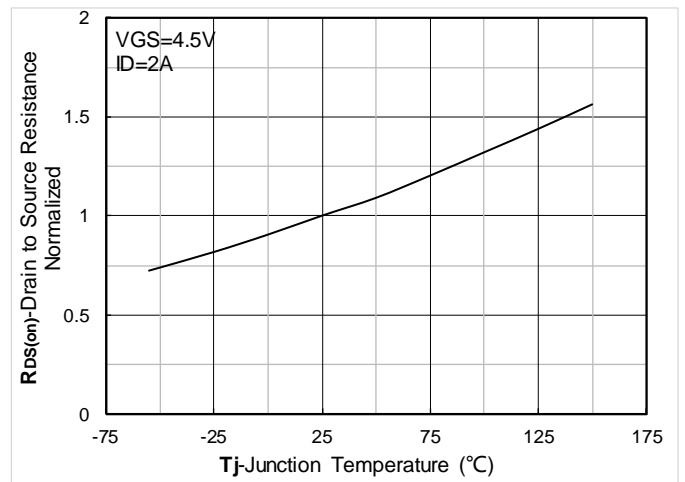


Figure 6. Normalized On-Resistance

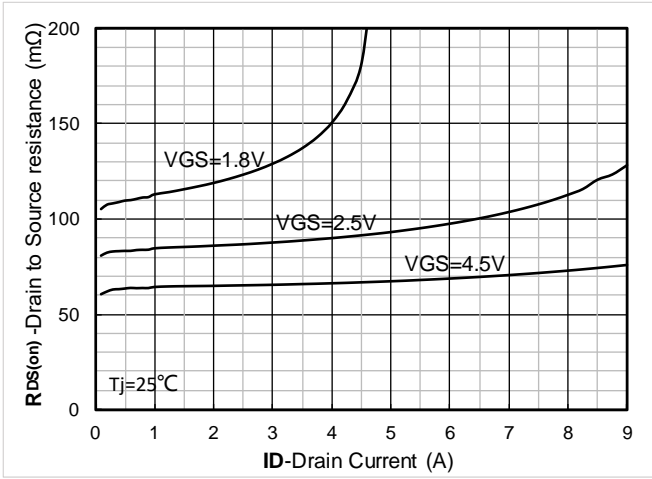


Figure 7. RDS(on) VS Drain Current; typical values

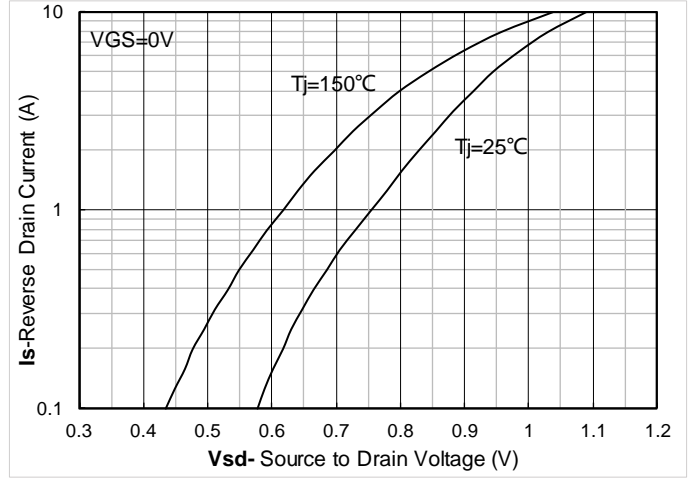


Figure 8. Forward characteristics of reverse diode; typical values

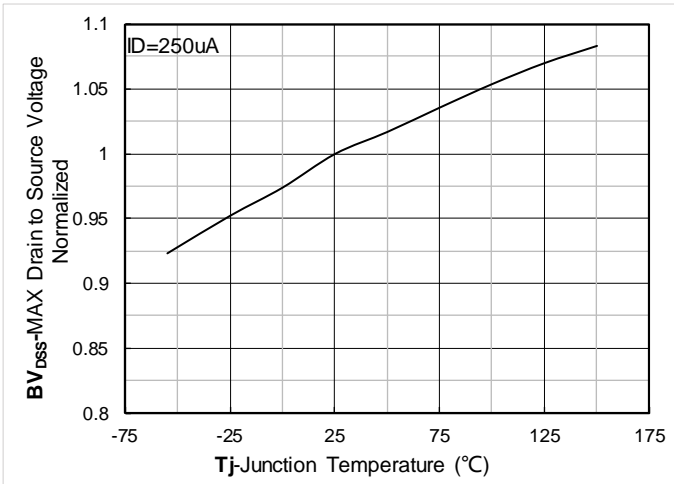


Figure 9. Normalized breakdown voltage

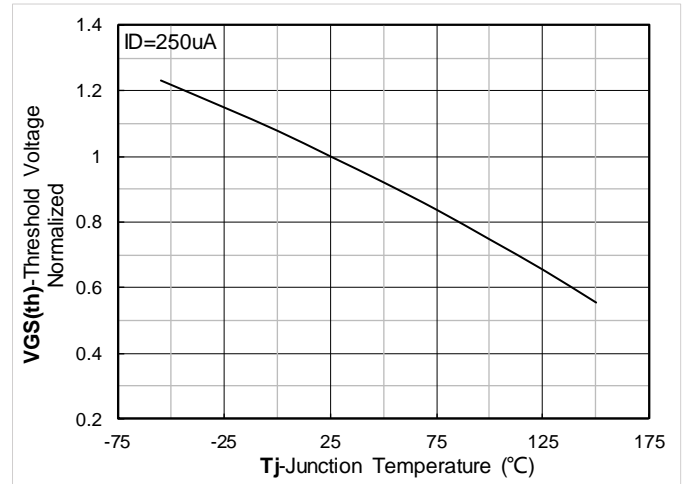


Figure 10. Normalized Threshold voltage

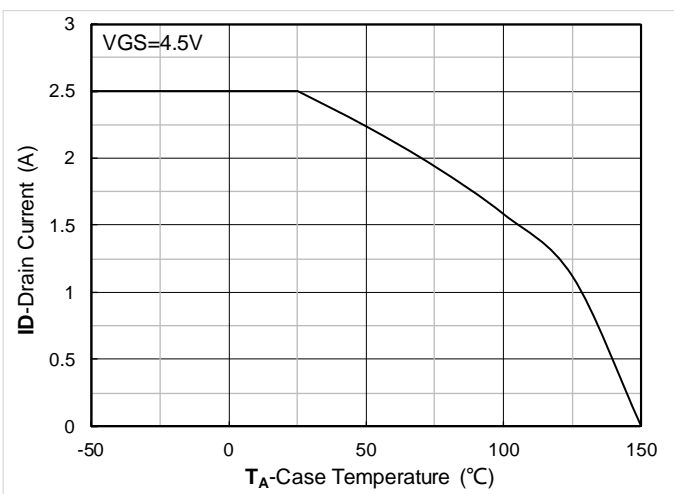


Figure 11. Current dissipation

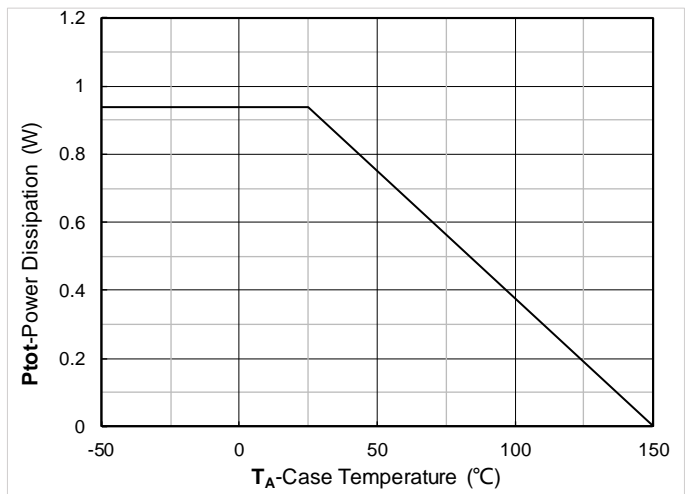


Figure 12. Power dissipation



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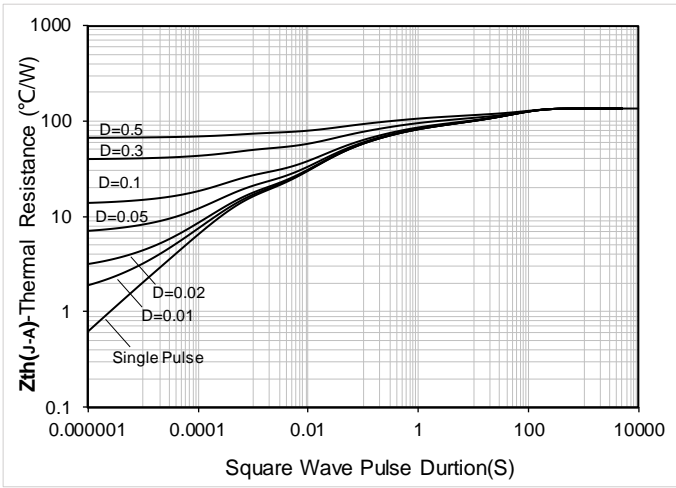


Figure 13. Maximum Transient Thermal Impedance

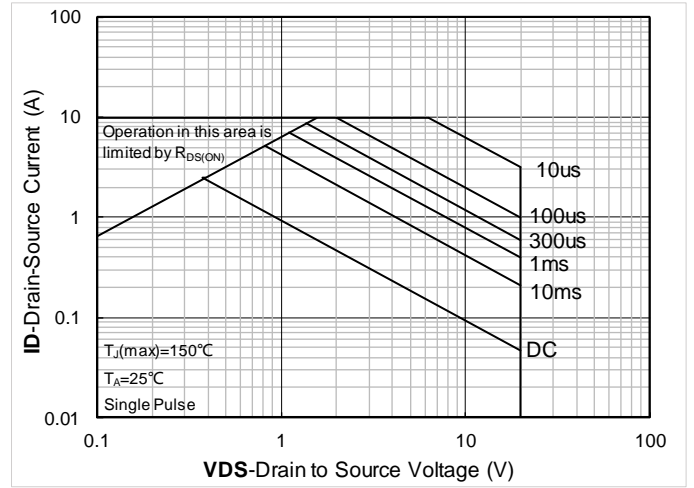


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

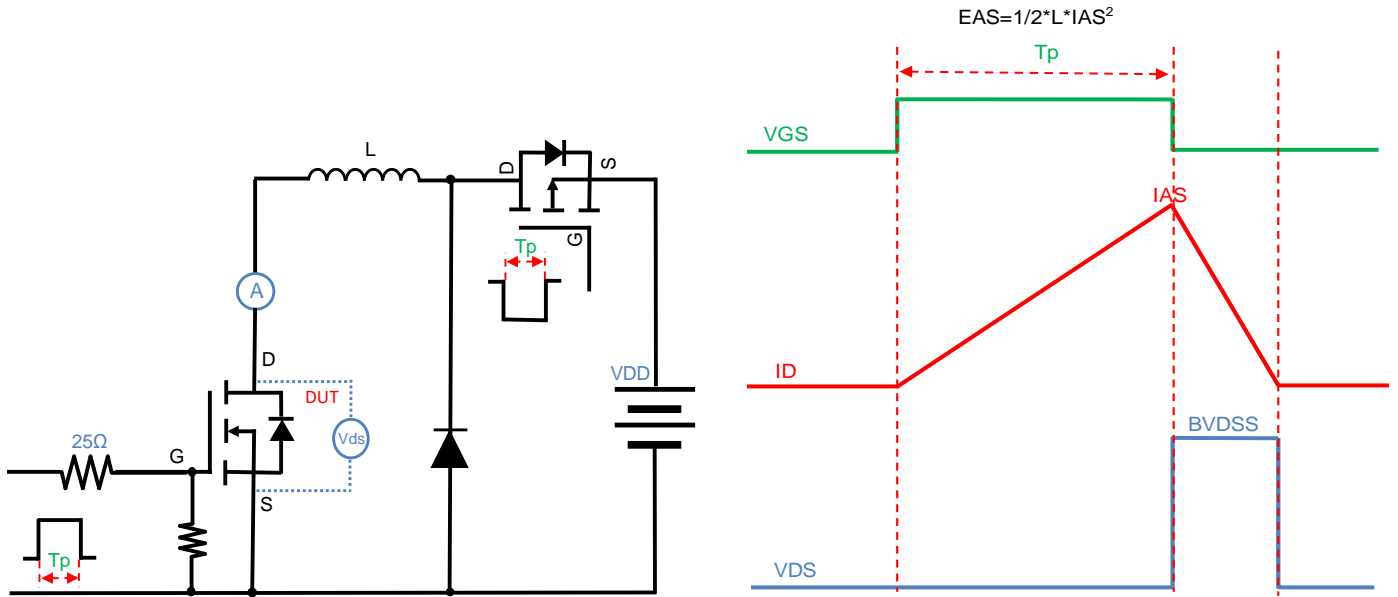


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

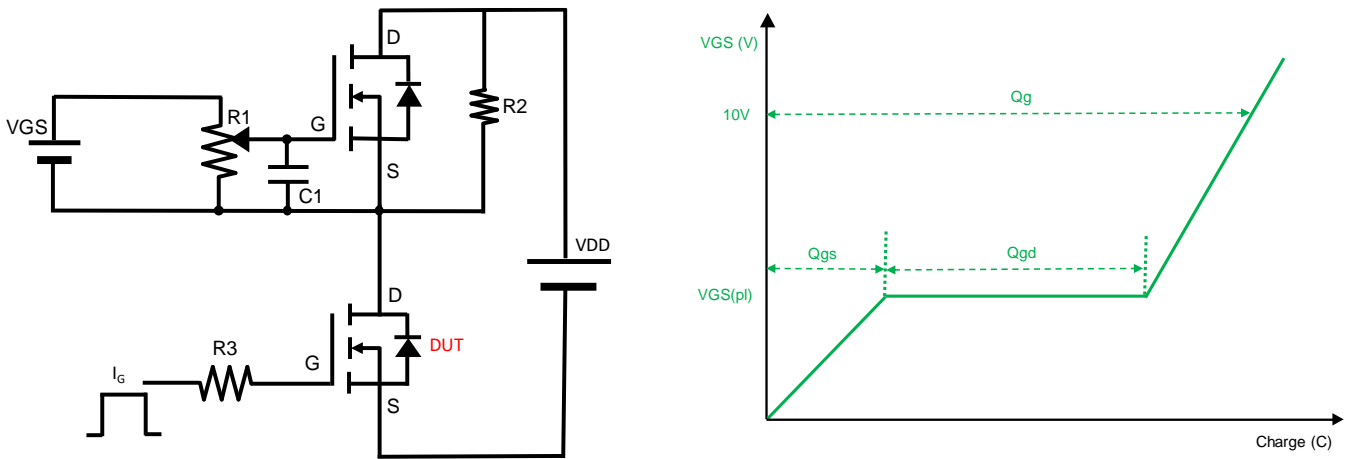


Figure B. Gate Charge Test Circuit & Waveform

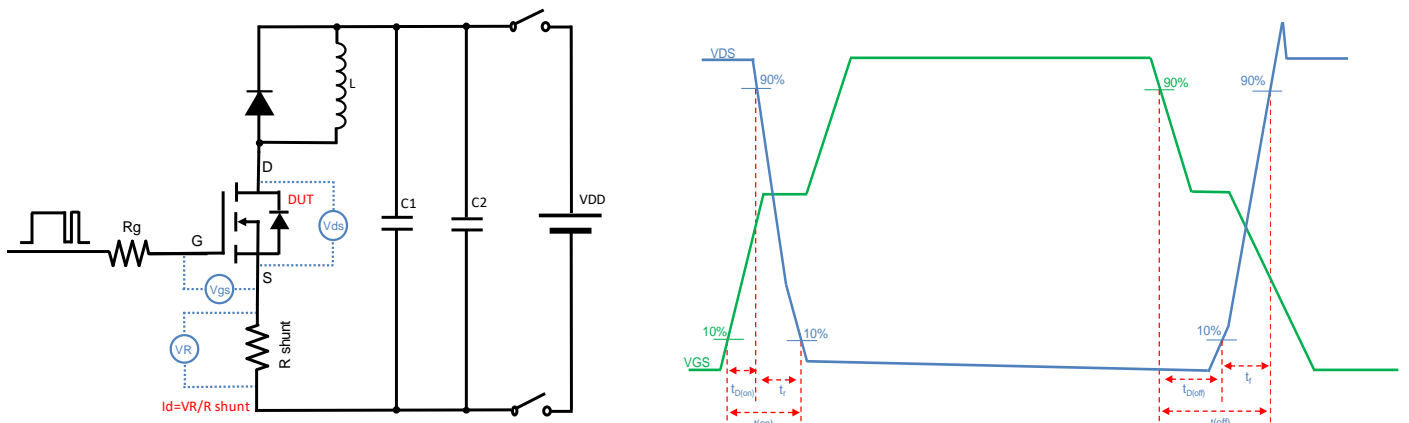


Figure C. Resistive Switching Test Circuit & Waveform

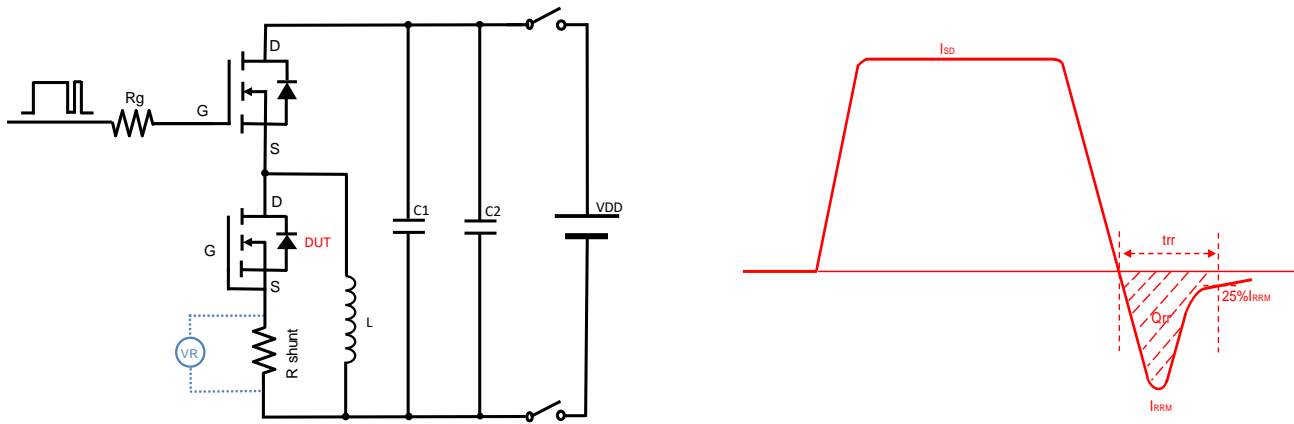
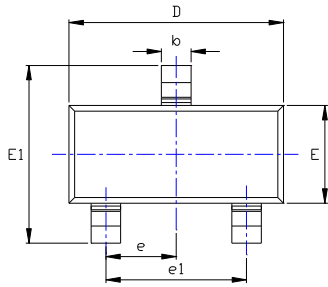


Figure D. Diode Recovery Test Circuit & Waveform

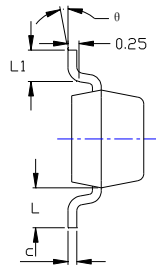


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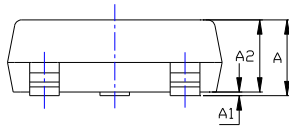
■ SOT-23 Package information



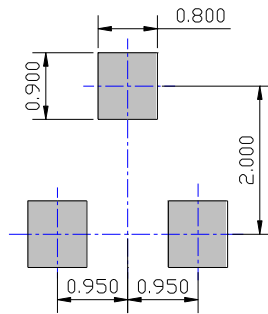
TOP VIEW



SIDE VIEW



SIDE VIEW



UNIT: mm

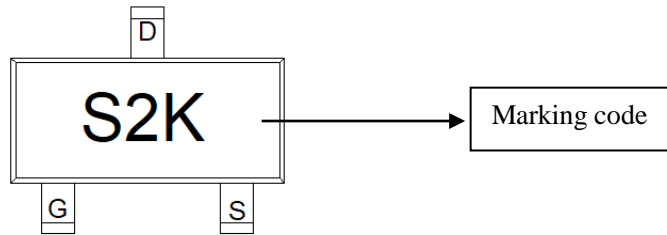
SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.045	0.900	1.150
A1	0.000	0.004	0.000	0.100
A2	0.035	0.041	0.900	1.050
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.110	0.118	2.800	3.000
E	0.047	0.055	1.200	1.400
E1	0.089	0.100	2.250	2.550
e	0.037TYP		0.950TYP	
e1	0.071	0.079	1.800	2.000
L	0.022REF		0.550REF	
L1	0.012	0.020	0.300	0.500
θ	0°	8°	0°	8°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



■Marking



Note:

1. All marking is at middle of the product body
2. All marking is in laser printing
3. S2K is marking code
4. Body color: Black



YJL2302AJK

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